IN THE CLAIMS:

Claims 1 (cancelled)

Claim 2 (cancelled)

Claim 3 (original) A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of memory sectors;

a control signal generation circuit, which generates a control signal;

a first signal buffer, which receives a read enable signal input from an external device;

an address buffer, which receives an address data input from the external device;

an address signal generation circuit, which generates an address signal in a predetermined order in synchronization with the control signal, and generates an address signal in a predetermined order based on the address data in synchronization with the read enable signal;

read means to select said memory sectors in said memory cell array based on the address data, and to read data from each of said plurality of flash memory cells of selected memory sectors;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, temporarily memorizes data read from said plurality of flash memory cells corresponding to selected memory sectors and receives an allocated address signal and outputs the data, which is temporarily memorized, read from said plurality of flash memory cells;

a data output buffer, which outputs the data, which is read from the said plurality of flash memory cells and output from said plurality of data memory circuits, to the external device in synchronization with the read enable signal; and

an error correction circuit, which receives the data, which is read from said plurality of flash

memory cells and output from said plurality of data memory circuits, in synchronization with the control signal, judges whether the data output from the data output buffer has an error in synchronization with the read enable signal, and corrects an error if there is the error.

Claim 4 (original) The flash memory according to claim 3, comprising a busy signal output circuit, which continuously outputs a busy signal to the external device for a period when data is read from the said plurality of flash memory cells and said error correction circuit receives data read from said plurality of flash memory cells.

Claim 5 (original) The flash memory according to claim 3, further comprising:

a command interface, which receives the status read instruction from the external device to generate a status read instruction signal; and

status output means to be activated by the status read instruction signal to output whether there is an error in the data read from said plurality of flash memory cells through the data output buffer.

Claim 6 (original) The flash memory according to claim 5, wherein said error correction circuit can correct a plurality of data in data read from said plurality of flash memory cells, and

said status output means can output the number of errors.

Claim 7 (original) The flash memory according to claim 5, wherein said error correction circuit can correct n data ($n \geq 1$) in the data read from said plurality of flash memory cells and can detect an existence of (n+1) errors, and

said status output means can output whether the error can be corrected.

Claims 8-14 (cancelled)

Claim 15 (currently amended) A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of memory sectors;

a control signal generation circuit, which generates a control signal;

a first signal buffer, which receives a read enable signal input from an external device;

an address buffer, which receives an address data input from the external device;

read means to select said memory sectors in said memory cell array based on the address data, and to read data from each of said plurality of flash memory cells of selected memory sectors;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, and temporarily memorizes the data read from said plurality of flash memory cells corresponding to said selected memory sector, and outputs the data read from said plurality of flash memory cells~~, which are temporarily memorized~~ in synchronization with the control signal and the read enable signal;

a data output buffer, which outputs the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits to the external device in synchronization with the read enable signal; and

an error correction circuit, which receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the control signal, judges whether the data output from the data output buffer has an error in synchronization with the read enable signal, and corrects the error if there is an error.

Claim 16 (original) The flash memory according to claim 15, comprising a busy signal output circuit, which continuously outputs a busy signal to the external device for a period when data is read from the said plurality of flash memory cells and said error correction circuit receives data

read from said plurality of flash memory cells.

Claim 17 (original) The flash memory according to claim 15, further comprising:

a command interface, which receives the status read instruction from the external device to generate a status read instruction signal; and

status output means to be activated by the status read instruction signal to output whether there is an error in the data read from said plurality of flash memory cells through the data output buffer.

Claim 18 (original) The flash memory according to claim 17 wherein

said error correction circuit can correct a plurality of data in data read from said plurality of flash memory cells, and

said status output means can output the number of errors.

Claim 19 (original) The flash memory according to claim 17, wherein

$(n \geq 1)$ in the data read from said plurality of flash memory cells and can detect an existence of (n+1) errors, and

said status output means can output whether the error can be corrected.

Claims 20-24 (cancelled)

Claim 25 (original) A flash memory comprising:

a memory sector with a plurality of flash memory cells;

a signal buffer, which receives a write enable signal input from an external device, and outputs a first control signal in a first period;

a control signal generation circuit, which generates a second control signal in a second period different from the first period;

a data input buffer, which receives a write data input from the external device in synchronization with the write enable signal;

an error correction circuit, which receives the write data in synchronization with the first control signal, and generates a check data for an error correction in synchronization with the second control signal;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, and takes the write data and the check data in synchronization with the first control signal and the second control signal and memorizes it temporarily;

means to write the write data and the check data, which are temporarily memorized in said plurality of data memory circuits, in said memory sector.

Claim 26 (original) The flash memory according to claim 25, further comprising a busy signal output circuit, which outputs busy signal to the external device in the second the period.

Claim 27 (original) A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of memory sectors;

a control signal generation circuit, which generates a first control signal in a first period;

signal buffer, which receives a read enable signal input from an external device, and outputs a second control signal in a second period different from the first period;

an address buffer, which receives an address data input from the external device;

read means to select said memory sectors in said memory cell array based on the address data, and to read data from each of said plurality of flash memory cells of selected memory sectors;

a plurality of data memory circuits, each of which is provided for each of said plurality of

flash memory cells, and temporarily memorizes the data read from said plurality of flash memory cells corresponding to said selected memory sector and outputs the data read from the memory cell, which temporarily memorizes it, in synchronization with the first control signal and the second control signal;

a data output buffer, which outputs the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, to the external device in synchronization with the second the signal;

an error correction circuit, which receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the first control signal, judges whether the data output from the data output buffer has an error in synchronization with the second the signal, and corrects the error if there is an error.

Claim 28 (original) The flash memory according to claim 27, comprising a busy signal output circuit, which continuously outputs a busy signal to the external device for a period when data is read from the said plurality of flash memory cells and said error correction circuit receives data from said plurality of flash memory cells.

Claim 29 (original) The flash memory according to claim 27, further comprising:

a command interface, which receives the status read instruction from the external device to generate a status read instruction signal; and

status output means to be activated by the status read instruction signal to output whether there is an error in the data read from said plurality of flash memory cells through the data output buffer.

Claim 30 (original) The flash memory according to claim 29, wherein

said error correction circuit can correct a plurality of data in data read from said plurality of flash memory cells, and

said status output means can output the number of errors.

Claim 31 (original) The flash memory according to claim 29, wherein

said error correction circuit can correct n data ($n \geq 1$) in the data read from said plurality of flash memory cells and can detect an existence of (n +1) errors, and

said status output means can output whether the error can be corrected.

Claim 32 (original) A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of memory sectors;

a signal buffer, which receives a read enable signal input from an external device, and outputs a first control signal in a first period;

a control signal generation circuit, which generates a second control signal in a second period different from the first period;

an address buffer, which receives the address data input from the external device;

read means to select said memory sectors in said memory cell array based on the address data, and to read data from each of said plurality of flash memory cells of selected memory sectors;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, temporarily memorizes the data read from said plurality of flash memory cells corresponding to said selected memory sector and outputs the data read from the memory cell, which temporarily memorizes it, in synchronization with the first control signal and the second control

signal;

a data output buffer, which outputs the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, to the external device in synchronization with the first control signal;

an error correction circuit, which receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the first control signal, receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the second control signal, judges whether there is an error in the data read from said plurality of flash memory cells, and specifies the data when there is an error.

Claim 33 (original) The flash memory according to claim 32, further comprising:

a command interface, which receives the status read instruction from the external device to generate a status read instruction signal; and

status output means to be activated by the status read instruction signal to output whether there is an error in the data read from said plurality of flash memory cells through the data output buffer.

Claim 34 (original) The flash memory according to claim 33, wherein

said error correction circuit can correct a plurality of data in data read from said plurality of flash memory cells, and

said status output means can output the number of errors.

Claim 35 (original) The flash memory according to claim 33, wherein

said error correction circuit can correct n data ($n \geq 1$) in the data read from said plurality of

flash memory cells and can detect an existence of (n+1) errors, and

said status output means can output whether the error can be corrected.

Claim 36 (original) The flash memory according to claim 32, further comprising a busy signal output circuit which outputs busy signal to the external device in a read period of data from the memory cell, and outputs a busy signal to the external device in the second period.

Claims 37-38 (cancelled).

Claim 39 (original) A flash memory comprising:

a memory sector with a plurality of flash memory cells;

a data buffer, which outputs a read data read from said memory sector to an external device;

an error correcting circuit, which output the read data from the data buffer and inputs the read data to specify an error read data from the read data, wherein

when the read data is output from said data buffer to the external device again, said error correction circuit corrects the error read data.

Claim 40 (original) The flash memory according to claim 39, further comprising a status output circuit which outputs an error state to the external device.

Claim 41 (original) The flash memory according to claim 39, further comprising a plurality of data memory circuits, which temporarily memorize to read data read from said memory sector.

Claims 42-50 (cancelled).

Claim 51 (newly added) A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of memory sectors;

a control signal generation circuit, which generates a control signal;

a first signal buffer, which receives a read enable signal input from an external device;

an address buffer, which receives an address data input from the external device;

an address signal generation circuit, which generates an address signal in a predetermined order in synchronization with the control signal, and generates an address signal in a predetermined order based on the address data in synchronization with the read enable signal;

a reader configured to select said memory sectors in said memory cell array based on the address data, and to read data from each of said plurality of flash memory cells of selected memory sectors;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, temporarily memorizes data read from said plurality of flash memory cells corresponding to selected memory sectors and receives an allocated address signal and outputs the data, which is temporarily memorized, read from said plurality of flash memory cells;

a data output buffer, which outputs the data, which is read from the said plurality of flash memory cells and output from said plurality of data memory circuits, to the external device in synchronization with the read enable signal; and

an error correction circuit, which receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the control signal, judges whether the data output from the data output buffer has an error in synchronization with the read enable signal, and corrects an error if there is the error.

Claim 52 (newly added) A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of memory sectors;

a control signal generation circuit, which generates a control signal;

a first signal buffer, which receives a read enable signal input from an external device;

an address buffer, which receives an address data input from the external device;

a reader configured to select said memory sectors in said memory cell array based on the address data, and to read data from each of said plurality of flash memory cells of selected memory sectors;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, and temporarily memorizes the data read from said plurality of flash memory cells corresponding to said selected memory sector, and outputs the data read from said plurality of flash memory cells[, which are temporarily memorized] in synchronization with the control signal and the read enable signal;

a data output buffer, which outputs the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits to the external device in synchronization with the read enable signal; and

an error correction circuit, which receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the control signal, judges whether the data output from the data output buffer has an error in synchronization with the read enable signal, and corrects the error if there is an error.

Claim 53 (newly added) A flash memory comprising:

a memory sector with a plurality of flash memory cells;

a signal buffer, which receives a write enable signal input from an external device, and outputs a first control signal in a first period;

a control signal generation circuit, which generates a second control signal in a second period different from the first period;

a data input buffer, which receives a write data input from the external device in synchronization with the write enable signal;

an error correction circuit, which receives the write data in synchronization with the first control signal, and generates a check data for an error correction in synchronization with the second control signal;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, and takes the write data and the check data in synchronization with the first control signal and the second control signal and memorizes it temporarily; and

a writer configured to write the write data and the check data, which are temporarily memorized in said plurality of data memory circuits, in said memory sector.

Claim 54 (newly added) A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of memory sectors;

a control signal generation circuit, which generates a first control signal in a first period;

signal buffer, which receives a read enable signal input from an external device, and outputs a second control signal in a second period different from the first period;

an address buffer, which receives an address data input from the external device;

a reader configured to select said memory sectors in said memory cell array based on the address data, and to read data from each of said plurality of flash memory cells of selected memory sectors;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, and temporarily memorizes the data read from said plurality of flash memory cells corresponding to said selected memory sector and outputs the data read from the memory cell, which temporarily memorizes it, in synchronization with the first control signal and the second control signal;

a data output buffer, which outputs the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, to the external device in synchronization with the second the signal;

an error correction circuit, which receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the first control signal, judges whether the data output from the data output buffer has an error in synchronization with the second the signal, and corrects the error if there is an error.

Claim 55 (newly added) A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of memory sectors;

a signal buffer, which receives a read enable signal input from an external device, and outputs a first control signal in a first period;

a control signal generation circuit, which generates a second control signal in a second period different from the first period;

an address buffer, which receives the address data input from the external device;

a reader configured to select said memory sectors in said memory cell array based on the address data, and to read data from each of said plurality of flash memory cells of selected

memory sectors;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, temporarily memorizes the data read from said plurality of flash memory cells corresponding to said selected memory sector and outputs the data read from the memory cell, which temporarily memorizes it, in synchronization with the first control signal and the second control signal;

a data output buffer, which outputs the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, to the external device in synchronization with the first control signal;

an error correction circuit, which receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the first control signal, receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the second control signal, judges whether there is an error in the data read from said plurality of flash memory cells, and specifies the data when there is an error.